LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit, comprising:

voltage generation means for generating a voltage on the basis of control data loaded into a data register;

nonvolatile storage means for holding the control data; and

a ~~processing circuit~~ controller used to generate the control data held in ~~said~~ the nonvolatile storage means, ~~said processing circuit~~ the controller being formed on one semiconductor substrate together with ~~said~~ the voltage generation means and ~~said~~ the nonvolatile storage means,

wherein ~~said processing circuit includes:~~

~~a decision circuit which determines~~ the controller obtains a relationship between a deciding reference voltage ~~supplied externally of the semiconductor substrate~~ and the voltage generated by ~~said~~ the voltage generation means, ~~; and~~

~~a control circuit which~~ determines the control data on the data register by referring to ~~an output from said~~

~~decision circuit~~the relationship, loads determined control data into the data register, and ~~which~~ stores the determined control data into ~~said~~ the nonvolatile storage means from the data register,

and ~~the operation of said control circuit is~~ an operation for obtaining the relationship and an operation for determining the control data are determined by a program.

2. (Currently Amended) The semiconductor integrated circuit according to claim 1,

wherein ~~said control circuit~~ the controller performs, in response to a first operation mode, a processing for determining control data on the data register by referring to the ~~output from said decision circuit~~ relationship and storing the determined control data in ~~said~~ the nonvolatile storage means by reading out the data from the data register, and performs, in response to a second operation mode, a processing for loading the control data from ~~said~~ the nonvolatile storage means into the data register.

3. (Currently Amended) The semiconductor integrated circuit according to claim 2, wherein ~~said control circuit~~ the controller comprises a central processing unit.

4. (Currently Amended) The semiconductor integrated circuit according to claim 3, further comprising a random access memory accessible by ~~said~~ the central processing unit,

wherein ~~said~~ the central processing unit executes, in response to the first operation mode, a program held in a predetermined area of ~~said~~ the random access memory.

5. (Currently Amended) The semiconductor integrated circuit according to claim 1,

wherein ~~said~~ the voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

6. (Currently Amended) The semiconductor integrated circuit according to claim 5,

wherein ~~said~~ the nonvolatile storage means comprises a flash memory, and said voltage generation means is capable of supplying a high voltage for erasing data in or writing data into ~~on~~ the flash memory.

7. (Currently Amended) A semiconductor integrated circuit, comprising:

a plurality of nonvolatile storage elements electrically erasable and writable;

voltage generation means for generating a high voltage for erase and write on ~~said~~ the plurality of nonvolatile storage elements on the basis of control data loaded into a data register from one of ~~said~~ the nonvolatile storage elements; and

a processing circuit used to generate the control data held in ~~said one of said~~ a nonvolatile storage ~~elements~~element, ~~said~~ the processing circuit being formed on one semiconductor substrate together with ~~said~~ the nonvolatile storage elements and ~~said~~ the voltage generation means,

wherein ~~said~~ the processing circuit ~~includes:~~

~~a decision circuit which determines the~~ obtains a relationship between a reference voltage ~~supplied externally of the semiconductor substrate~~ and the voltage generated by ~~said~~ the voltage generation means, ~~; and~~

~~a control circuit which~~ determines the control data by referring to ~~an output from said decision circuit~~the relationship, loads a determined control data into the data register, and then stores the determined control data into

the nonvolatile storage element,

and ~~the operation of said control circuit is~~ an operation for obtaining the relationship and an operation for determining the control data are determined by a program.

8. (Currently Amended) The semiconductor integrated circuit according to claim 7,

wherein ~~said control circuit~~ the processing circuit performs, in response to a first operation mode, processing for determining control data on the data register by referring to the ~~output from said decision circuit~~ relationship and storing the determined control data in ~~said one of said~~ the nonvolatile storage ~~elements~~ element by reading out the data from the data register, and performs, in response to a second operation mode, processing for loading the control data from ~~one of said~~ the nonvolatile storage ~~elements~~ element into the data register.

9. (Currently Amended) The semiconductor integrated circuit according to claim 7,

wherein ~~said~~ the voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

10. (Currently Amended) The semiconductor integrated circuit according to claim 9,

wherein ~~said~~ the nonvolatile storage element is a flash memory element, and ~~said~~ the voltage generation means is capable of supplying a high voltage ~~for~~ to erase ~~and~~ data in or write ~~on~~ data into the flash memory element.

11. (Currently Amended) A semiconductor integrated circuit, comprising:

a clock generation circuit which provides a clock signal having a signal cycle according to control data loaded into a data register;

nonvolatile storage means for holding the control data; and

a processing circuit used to generate the control data held in ~~said~~ the nonvolatile storage means, ~~said~~ the processing circuit being formed on one semiconductor substrate together with ~~said~~ the clock generation circuit and ~~said~~ the nonvolatile storage means,

wherein ~~said~~ the processing circuit ~~includes:~~

~~a decision circuit which determines~~ obtains a relationship between the pulse width of a reference pulse signal and the pulse width of the clock signal generated by

~~said~~ the clock generation circuit, ~~; and~~

~~a control circuit which~~ determines the control data on the data register by referring to ~~an output from said decision circuit~~the relationship, loads a determined control data into the data register, and stores the determined control data into the nonvolatile storage means,

and ~~the operation of said control circuit is~~ an operation for obtaining the relationship and an operation for determining the control data are determined by a program.

12. (Currently Amended) The semiconductor integrated circuit according to claim 11,

wherein ~~said~~ the clock generation circuit includes an oscillation circuit, and a frequency dividing circuit which divides the frequency of an oscillation signal output from ~~said~~ the oscillation circuit on the basis of the control data loaded into the data register.

13. (Currently Amended) The semiconductor integrated circuit according to claim 12,

wherein ~~said~~ the control circuit stores the determined control data in ~~said~~ the nonvolatile storage means.

14. (Currently Amended) The semiconductor integrated circuit according to claim 13,

wherein ~~said control circuit~~ the processing circuit performs, in response to a first operation mode, processing for determining the control data with reference to the ~~output from said decision circuit~~ relationship and storing the determined control data in ~~said~~ the nonvolatile storage means, and performs, in response to a second operation mode, processing for loading the control data from ~~said~~ the nonvolatile storage means into the data register.

15. (Currently Amended) The semiconductor integrated circuit according to claim 14,

wherein ~~said control~~ the processing circuit comprises a central processing unit.

16. (Currently Amended) The semiconductor integrated circuit according to claim 15, further comprising a random access memory accessible by ~~said~~ the central processing unit,

wherein ~~said~~ the central processing unit executes, in response to the first operation mode, a program held in a predetermined area of ~~said~~ the random access memory.

17. (Currently Amended) The semiconductor integrated circuit according to claim 16,

wherein the clock signal generated from ~~said~~ the clock generation circuit is a write control clock signal; ~~said~~ the nonvolatile storage means comprises a flash memory; and ~~said~~ the write control clock signal determines the pulse width of a write pulse for writing to the flash memory.

18. (Currently Amended) A method of testing a plurality of semiconductor integrated circuits in a parallel manner, each semiconductor integrated circuit having voltage generation means capable of generating a voltage on the basis of control data loaded into a data register, nonvolatile storage means in which the control data is held, a processing circuit used to prepare the control data held in the nonvolatile storage means, the processing circuit being formed on one semiconductor substrate together with the voltage generation means and the nonvolatile storage means, said method comprising:

a first process ~~comprising~~ including a step of inputting a reference voltage to the plurality of semiconductor integrated circuits from the outside in a parallel manner; and

a second process ~~comprising~~ including the steps of:

in execution of a test operation by means of the processing circuit of each semiconductor integrated circuit, determining a relationship between the voltage generated by the voltage generation means and the reference voltage on the basis of control data set in the data register;

updating the control data until a target condition is reached by the determination result; and

storing the control data in the nonvolatile storage means when the target condition is reached by the determination result.

19. (Currently Amended) The method of testing a plurality of semiconductor integrated circuits according to claim 18, further comprising a third process including loading a test program into each semiconductor integrated circuit,

wherein said second process includes the steps of:

making ~~said~~ the determination by using a decision circuit in the processing circuit; and

making a central processing unit in the processing circuit execute the test program to update the control data and to store the control data in the nonvolatile storage means.

20. (Original) The method of testing a plurality of semiconductor integrated circuits according claim 18, wherein the voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

21. (Currently Amended) The method of testing a plurality of semiconductor integrated circuits according to claim 20,

wherein the nonvolatile storage means comprises a flash memory, and the voltage generation means is capable of supplying a high voltage ~~for~~ to erase data in or ~~and~~ write ~~on~~ data into the flash memory.

22. (Currently Amended) A method of testing a plurality of semiconductor integrated circuits in a parallel manner, each semiconductor integrated circuit having an oscillation circuit, a frequency dividing circuit which controls the ratio of division of the frequency of an oscillation signal output from the oscillation circuit on the basis of ~~a~~ control data loaded into a data register, nonvolatile storage means for storing the control data, and a processing circuit used to generate the control data held in the nonvolatile storage means, said processing circuit

being formed on one semiconductor substrate together with the oscillation circuit, the frequency dividing circuit, and the nonvolatile storage means, said method comprising:

a first process ~~comprising~~ including the step of instructing each of the plurality of semiconductor integrated circuits to execute a test operation; and

a second process ~~comprising~~ including the steps of:

in execution of the test operation by means of the processing circuit of each semiconductor integrated circuit, determining a relationship between the pulse width of a periodic signal generated by the frequency dividing circuit and the pulse width of a reference pulse signal on the basis of the control data set in the data register;

updating the control data until a target condition is reached by the determination result; and

storing the control data in the nonvolatile storage means when the target condition is reached by the determination result.

23. (Currently Amended) The method of testing a plurality of semiconductor integrated circuits according to claim 22, further comprising a third process ~~comprising~~ including the step of loading a test program into each semiconductor integrated circuit,

wherein said second ~~processing comprises~~ process includes the steps of:

making ~~said~~ the determination by using a decision circuit in the processing circuit; and

making a central processing unit in the processing circuit execute the test program to update the control data and to store the control data in the nonvolatile storage means.